

**ARM ISA Multiple Choice Questions**

Based on the ARM Instruction Set Architecture document, here are 15 multiple-choice questions covering key concepts:

**Questions**

**1. Which ARM processor family is specifically designed for microcontroller applications and is cost-sensitive?**  
a) ARM Cortex-A family  
b) ARM Cortex-R family  
c) ARM Cortex-M family  
d) ARM Cortex-X family

**2. What is the bit width of each register in ARM Cortex-M processors?**  
a) 16 bits  
b) 24 bits  
c) 32 bits  
d) 64 bits

**3. Which registers are considered "Low Registers" in ARM Cortex-M and can be accessed by any instruction?**  
a) R0-R7  
b) R8-R12  
c) R13-R15  
d) R0-R12

**4. What does the R15 register represent in ARM architecture?**  
a) Stack Pointer  
b) Link Register  
c) Program Counter  
d) Status Register

**5. Which instruction set was first introduced in ARM7TDMI processors in 1995?**  
a) ARM32  
b) Thumb-1 (16-bit Thumb)  
c) Thumb-2  
d) ARM64

**6. In ARM assembly instruction format, what is typically the first operand (operand1)?**  
a) Source register  
b) Immediate value  
c) Destination register  
d) Memory address

**7. Which assembly directive is used to allocate one or more 32-bit words of data?**  
a) DCB  
b) DCW  
c) DCD  
d) DCQ

**8. How many ENTRY directives must be present in an ARM assembly application?**  
a) Zero  
b) Exactly one  
c) At least one per source file  
d) One per subroutine

**9. What does the EXPORT directive do in ARM assembly?**  
a) Imports symbols from other files  
b) Declares a symbol and makes it visible to the linker  
c) Defines the end of a procedure  
d) Allocates memory space

**10. Which two stack pointers does ARM Cortex-M4 support?**  
a) MSP and LSP  
b) PSP and LSP  
c) MSP and PSP  
d) SSP and USP

**11. What is the purpose of the Load-Modify-Store operation pattern in ARM assembly?**  
a) To handle interrupts  
b) To manage memory alignment  
c) To translate C operations to assembly (load values from memory, modify in registers, store results)  
d) To implement branch predictions

**12. Which directive pair is used to mark the start and end of a function in ARM assembly?**  
a) AREA and END  
b) PROC and ENDP  
c) ENTRY and EXIT  
d) START and STOP

**13. What type of access do peripheral registers use in ARM Cortex-M processors?**  
a) Direct register access  
b) Memory-mapped I/O  
c) Port-mapped I/O  
d) Interrupt-driven access

**14. Which assembly directive is used to give a symbolic name to a register?**  
a) EQU  
b) RN  
c) EXPORT  
d) IMPORT

**15. What does the ALIGN directive accomplish in ARM assembly?**  
a) Sets register values to zero  
b) Aligns data or code to a particular memory boundary  
c) Imports external symbols  
d) Defines constant values

**Answer Key**

1. **c) ARM Cortex-M family** - The document states that ARM Cortex-M family is for microcontrollers and is cost-sensitive[[1]](#fn1)
2. **c) 32 bits** - Each register has 32 bits according to the document[[1]](#fn1)
3. **a) R0-R7** - Low Registers R0-R7 can be accessed by any instruction[[1]](#fn1)
4. **c) Program Counter** - R15 is the Program Counter (PC) that contains the memory address of the current instruction[[1]](#fn1)
5. **b) Thumb-1 (16-bit Thumb)** - 16-bit Thumb was first used in ARM7TDMI processors in 1995[[1]](#fn1)
6. **c) Destination register** - Normally operand1 is the destination register[[1]](#fn1)
7. **c) DCD** - DCD (Define Constant Word) allocates 32-bit words[[1]](#fn1)
8. **b) Exactly one** - There must be exactly one ENTRY directive in an application[[1]](#fn1)
9. **b) Declares a symbol and makes it visible to the linker** - EXPORT declares a symbol and makes it visible to the linker[[1]](#fn1)
10. **c) MSP and PSP** - Cortex-M4 supports Main SP (MSP) for privileged access and Process SP (PSP) for application access[[1]](#fn1)
11. **c) To translate C operations to assembly (load values from memory, modify in registers, store results)** - This is the standard pattern for translating C to assembly[[1]](#fn1)
12. **b) PROC and ENDP** - PROC and ENDP mark the start and end of a function/subroutine[[1]](#fn1)
13. **b) Memory-mapped I/O** - Processor accesses peripheral registers via memory-mapped I/O[[1]](#fn1)
14. **b) RN** - The RN directive gives a symbolic name to a specific register[[1]](#fn1)
15. **b) Aligns data or code to a particular memory boundary** - ALIGN directive aligns data or code to particular memory boundaries[[1]](#fn1)

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